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EXAMINER	
TRAN, DZUNG D	

ART UNIT	PAPER NUMBER
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/941,557	BAKER ET AL.	
	Examiner	Art Unit	
	Dzung D. Tran	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12,14-25,27-36,38,40,44-53,56-69,71-82,84,88-89,91,95,97-98,100-108,111-115,117-120,122,126-133,136-140,142-145,147 and 151-163* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-9,12,14-25,27-36,38,40,44-53,56-69,71-82,84,88,89,91,95,97,98,100-108,111-115,117-120,122,126-133,136-140,142-145,147 and 151-163.

DETAILED ACTION

Specification

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 12, 14, 27-29, 31, 35, 44, 73, 75-76, 79, 89, 91, 95, 97-98, 100-104, 117, 120, 126-129, 142 and 145 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozeki et al. US patent no. 6,651,139 in view of Shimura et al. US patent no. 7,133,610.

Regarding claims 1, 27, 117 and 142 Ozeki discloses in figure 6 a communication bus system between processors and memory modules comprising:

a memory controller 11 (i.e. Processor 11a, 11b, 11c...);

at least one memory storage device 15 (i.e., cache memory) connected to memory bus (i.e., the bus from interface 14 to cache memory 15); and

a continuous optical path 13 coupled to said memory controller 11 and to memory bus arranged and configured for exchanging data between said memory controller 11 and said at least one memory storage device 15, said optical path 13 arranged and configured to convert an electrical signal output from said controller to an optical signal (i.e., by electric/optical conversion unit 21; col. 5, lines 9-10) for

transmission on said continuous optical path 13, said memory controller 11, memory bus 15 and continuous optical path 13 being formed on a single die.

Ozeki does not specifically disclose a wavelength sensing mechanism connected to said controller arranged and configured to provide wavelength information with respect to an optical signal on said optical path. Shimura discloses in Figure 5, a wavelength sensing mechanism 22 (i.e. wavelength monitor) connected to a controller (i.e., wavelength supervisory circuit 58) and configured to provide wavelength information with respect to an optical signal on said optical path (See figure 5).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to include the wavelength sensing and controlling part taught by Shimura in the system of Ozeki. One of ordinary skill in the art would have been motivated to do in order to detect and adjust the optical wavelength of the optical signal.

Regarding claim 2, Ozeki discloses memory controller 11 transmits data to said at least one memory storage device 16 through said optical path 13 (col. 5, lines 1-20).

Regarding claim 3, Ozeki discloses memory controller 11 and said at least one data includes at least one of memory device 16 are arranged and configured to exchange read/write data (col. 5, lines 42-65).

Regarding claim 4, Ozeki discloses the continuous optical path includes at least one optical link 13 for exchange read/write data (col. 5, lines 42-65).

Regarding claim 5, Ozeki discloses data includes address data transmitted from said memory controller 11 to said at least one memory storage device 16 (col. 8, lines 16-20).

Regarding claims 89, 101 and 126, Ozeki disclose in Figure 3, an electro-optical converter 21 comprising:

at least one input (i.e., electrical input) arranged and configured to receive an electrical data signal from a memory controller 11;

at least one optical output (i.e., to light signal) arranged and configured to transmit said optical signal into optical path 13.

Regarding claims 12 and 14, Ozeki discloses an electro-optical converter 22 for converting an optical signal on said optical path 13 to an electrical signal and transmitting said electrical signal to said controller 11 and memory storage device.

Regarding claims 97 and 100, Ozeki discloses an optical receiver 22 includes a photodiode 28 (see Figure 3).

Regarding claims 102 and 127, Ozeki discloses controller receives data from said at least one memory storage device through said optical path 13 (col. 5, lines 1-20).

Regarding claims 103 and 128, Ozeki discloses data includes at least one of read and write data (col. 5, lines 42-65).

Regarding claims 104 and 129, Ozeki discloses data includes address data transmitted from said controller to said at least one memory device (col. 8, lines 16-20).

Regarding claim 44, Ozeki discloses memory module comprises an electro-optical converter 22 of figure 3 for connecting optical data from said optical path 13 to electrical signals for said at least one memory device from the node.

Regarding claims 29, 73 and 76, Ozeki discloses in figure 6, a single optical path 13 between said controller 11 and at least one memory device 16 for exchanging at least read/write data (col. 5, lines 42-65) present on a plurality of electrical paths (figures 3, 6) between said controller 11 and at least one memory storage device 16.

Regarding claims 31, 35, 75, 79, 120 and 145, Ozeki discloses single optical path 13 further arranged and configured to exchange data includes address data transmitted from said controller to said at least one memory device (col. 5, lines 1-20).

Regarding claim 91, Ozeki discloses transmitter 21 include laser optical source (LD 25 of Figure 3).

Regarding claims 95 and 98, Ozeki discloses optical receiver 22 (same as an electro-optical converter) at least one input for receiving a optical data signal from an optical path 13; at least one electro-optical converter 28 for converting said received data signal to an electrical signal and at least one electrical output for transmitting said output signal to an electrical path of a memory controller 11 or memory device from the node.

3. Claims 6-8, 24-25, 30, 32-34, 36, 38, 40, 45-51, 53, 56, 58, 68-69, 71-85, 88, 106-107, 115, 118-119, 122, 131-132, 139, 140, 144, 147, 151, 155 and 159 are

rejected under 35 U.S.C. 103(a) as being unpatentable over Ozeki et al. US patent no. 6,651,139 in view of Shimura et al. US patent no. 7,133,610 and further in view of Acton et al. US patent no. 5,544,319.

Regarding claims 6, 105 and 130, as per claims above, the combination of Ozeki and Shimura discloses all the limitations except for data includes command data transmitted from said controller to said at least one memory storage device. Acton, from the same field of endeavor, discloses data includes command data transmitted from said controller to said at least one memory storage device (col. 16, lines 20-22).

At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to include the teaching of Acton in the system of Ozeki and Shimura. One of ordinary skill in the art would have been motivated to do in order to control the information between the memory controller and the memory storage device.

Regarding claim 7, Acton discloses optical path 4 includes an optical link for transmission a clock signal (col. 9, lines 50- 51).

Regarding claim 8, Acton discloses optical path 4 includes an optical link for transmission control data (figure 4, col. 6, line 24).

Regarding claim 45, Acton discloses a processor (col. 2, line 47);

Regarding claims 46 and 47, Ozeki discloses controller 11 for exchange data to and from said at least one memory storage device from the node through said optical path 13 (see figure 6).

Regarding claim 48, Ozeki discloses optical path 13 includes at least one optical link for exchange of read and write data (col. 5, lines 42-65).

Regarding claim 49, Ozeki discloses optical path 4 includes an optical link for address data transmitted from said controller to said at least one memory storage device (col. 8, lines 16-20).

Regarding claims 56, 58 and 88, Ozeki discloses optical receiver 22 (same as an electro-optical converter) for converting an optical signal on said optical path 13 to an electrical signal and transmitting said electrical signal to said controller 11.

Regarding claims 71-72, Ozeki discloses in Figure 3, wavelength sensing mechanism (e.g., arbitrary light intensity) connect to controller 11 arranged and configured to provide wavelength information to said controller 11 and wherein said wavelength sensing mechanism (e.g., arbitrary light intensity) is located at a controller side and controller 11 is arranged to provide wavelength adjustment to said LD 25 (col. 6, lines 31-36).

Regarding claims 106 and 131, Acton discloses data includes a clock signal (col. 9, lines 50- 51).

Regarding claims 107 and 132, Acton discloses data includes control data (figure 4, col. 6, line 24).

Regarding claims 24, 68 and 139, Acton discloses at least one memory device is located memory coupled system (e.g. same as a memory module) (col. 2, lines 44-48).

Regarding claims 25, 69, 115 and 140, Acton discloses the bus 5 of each memory coupled system is connected to an optical fiber 4 to memory coupling system controller (col. 2, lines 48-50).

Regarding claim 30, 34, 74, 78, 119 and 144, Acton discloses single optical path 4 further arranged and configured to exchange data includes command data transmitted from said controller to said at least one memory device (col. 16, lines 20-22).

Regarding claims 32, 36, 80 and 81, Acton discloses single optical path 4 further arranged and configured to exchange data includes a clock signal (col. 9, lines 50- 51).

Regarding claims 33, 77, 118 and 143, Acton discloses in figures 2 and 3, data includes read/write data which originates on a plurality of electrical paths, said optical path 4 comprising a plurality of discrete optical guides respectively associated with said electrical path (col. 3, lines 22-30).

Regarding claims 38 and 82, Acton discloses data includes control data (figure 4, col. 6, line 24).

Regarding claims 40, 84, 122 and 147, Acton discloses in figure 1, a processor (col. 2, line 47) for communicating with said at least one memory device, wherein said controller 1, at least one memory device, processor, and optical path are all integrated on the same die (figure 1).

Regarding claim 50, Acton discloses optical path 4 includes an optical link for command data transmitted from said controller to said at least one memory storage device (col. 16, lines 20-22).

Regarding claim 51, Acton discloses optical path 4 includes an optical link for transmission a clock signal (col. 9, lines 50- 51).

Regarding claim 52, Acton discloses optical path 4 includes an optical link for transmission control data (figure 4, col. 6, line 24).

Regarding claims 151, 155 and 159, multiplexed optical channels use TDM is well known in the art (for example SONET system).

4. Claims 9, 15-23, 52, 59-67, 108, 111-113, 133, 136-138, 152-154, 156-158 and 160-163 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozeki et al. US patent no. 6,651,139 in view of Shimura et al. US patent no. 7,133,610 and Acton et al. US patent no. 5,544,319 and further in view of Fee US Patent no. 6,658,210.

Regarding claims 9, 52, 108, 133 and 163, as per claims above, the combination of Ozeki, Acton and Shimura discloses all the limitations except for optical path comprises a plurality of multiplexed optical channels, said data being transmitted over said multiplexed optical channels. Fee discloses a WDM optical system comprising a bi-directional optical fiber has a plurality wavelengths to carry information (abstract) and data being transmitted over multiplexed optical channels (e.g. WDM, see col. 2, lines 47-55). At the time of the invention was made, it would have been obvious to a person

of ordinary skill in the art to incorporated WDM coupler for multiplexing and de-multiplexing optical signals of Fee in the combination of Ozeki, Acton and Shimura. One of ordinary skill in the art would have been motivated to do this since Wavelength Division Multiplexing Multiplex/Demultiplex coupler offers advantages of allowing the optical signals transmits back and forth over an bi-directional optical link and allow multi-wavelengths to communicate via single fiber or wave guide.

Regarding claims 15, 59, 111, 112, 136 and 137, the combination of Ozeki and Shimura and Fee discloses a multiplexer/demultiplexe (220 of figure 3 of Fee) associated with said controller for multiplexing said optical channels, and associated with said at least one memory device for demultiplexing said multiplexed optical channels.

Regarding claims 16 and 60, the combination of Ozeki and Shimura and Fee discloses a multiplexer/demultiplexe (226 of figure 3 of Fee) associated with said at least one memory device for multiplexing optical channels and providing multiplexed optical channels to said optical path 4 and associated with said memory controller for demultiplexing said multiplexed optical channels.

Regarding claims 17, 61, 113 and 138, the combination of Ozeki and Shimura and Fee discloses a multiplexer/demultiplexe (220, 226 of figure 3 of Fee) located on each side of said optical path.

Regarding claims 18 and 62, Acton discloses data includes at least one of read and write data (abstract, col. 2, lines 48-51).

Regarding claims 19 and 63, Acton discloses data includes command data transmitted from said controller to said at least one memory device (col. 16, lines 20-22).

Regarding claims 20 and 64, Acton discloses data includes address data transmitted from said controller to said at least one memory device (figure 3, col. 3, line 49, col. 5, lines 54-62).

Regarding claims 21 and 65, Acton discloses data includes a clock signal (col. 9, lines 50- 51).

Regarding claims 22 and 66, Acton discloses data includes control data (figure 4, col. 6, line 24).

Regarding claims 23 and 67, Acton discloses electrical paths connected between said controller 1 and said at least one memory device 5 for passing data between said controller and memory device (see figure 3).

Regarding claims 152-155, 156-157, 160 and 161, Fee discloses multiplexed optical channels use WDM (see col. 2, lines 47-55).

Regarding claims 154, 158 and 162, transmitting compressed data is well known in the art.

Response to Arguments

5. Applicant's arguments filed on 05/01/2008 have been fully considered but they are not persuasive.

A) Rejection 1-5, 12, 14, 27-29, 31, 35, 44, 73, 75-76, 79, 89, 91, 95, 97-98, 100-104, 117, 120, 126-129, 142 and 145 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozeki et al. US patent no. 6,651,139 in view of Shimura et al. US patent no. 7,133,610.

Applicant argues that Ozeki does not disclose a memory bus. Examiner submits that in the new rejection, Examiner clearly indicates that Ozeki discloses in figure 6, a memory controller 11 (i.e. Processor 11a, 11b, 11c...) and at least one memory storage device 15 (i.e., cache memory) connected to memory bus (i.e., the bus from interface 14 to cache memory 15). Examiner further used Shimura reference that teaches the missing limitation wavelength sensing mechanism (i.e. wavelength monitor 22).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dzung Tran whose telephone number is (571) 272-3025.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jason Chan, can be reached on (571) 272-3022.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Dzung Tran

07/15/2008

/Dzung D Tran/

Primary Examiner, Art Unit 2613